

## LP38512-1.8

# 1.5A Fast-Transient Response Low-Dropout Linear Voltage Regulator with Error Flag

### General Description

The LP38512-1.8 Fast-Transient Response Low-Dropout Voltage Regulator offers the highest-performance in meeting AC and DC accuracy requirements for powering Digital Cores. The LP38512-1.8 uses a proprietary control loop that enables extremely fast response to change in line conditions and load demands. Output Voltage DC accuracy is guaranteed at 2.5% over line, load and full temperature range from -40°C to +125°C. The LP38512-1.8 is designed for inputs from the 2.5V, 3.3V, and 5.0V rail, is stable with 10  $\mu$ F ceramic capacitors, and has a fixed 1.8V output. An Error Flag feature monitors the output voltage and notifies the system processor when the output voltage falls more than 15% below the nominal value. The LP38512-1.8 provides excellent transient performance to meet the demand of high performance digital core ASICs, DSPs, and FPGAs found in highly-intensive applications such as servers, routers/switches, and base stations.

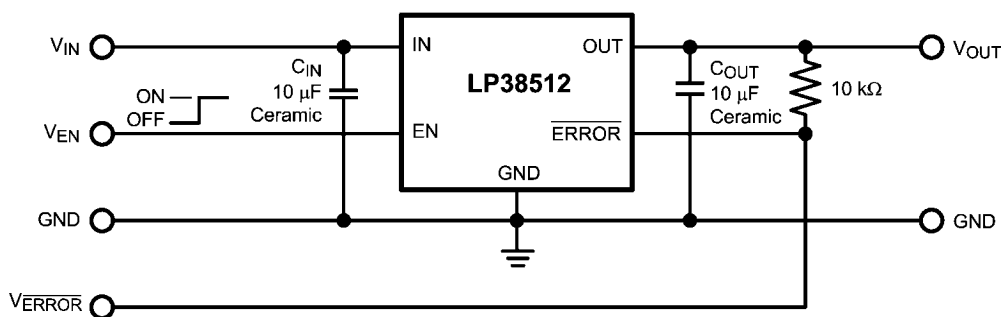
### Features

- 2.25V to 5.5V Input Voltage Range
- 1.8V Fixed Output Voltage
- 1.5A Output Load Current
- $\pm 2.5\%$  Accuracy over Line, Load, and Full-Temperature Range from -40°C to +125°C
- Stable with tiny 10  $\mu$ F ceramic capacitors
- 0.20% Output Voltage Load Regulation from 10 mA to 1.5A
- Enable pin
- $\overline{\text{Error}}$  Flag Indicates Status of Output Voltage
- 1 $\mu$ A of Quiescent current in Shutdown
- 40dB of PSRR at 100 kHz
- Over-Temperature and Over-Current Protection
- TO-263 and TO-263 THIN Surface Mount Packages

### Applications

- Digital Core ASICs, FPGAs, and DSPs
- Servers
- Routers and Switches
- Base Stations
- Storage Area Networks
- DDR2 Memory

### Typical Application Circuit



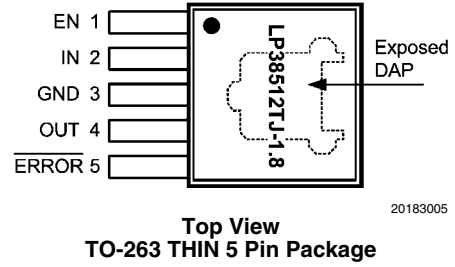
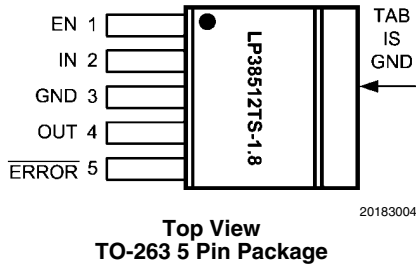
20183001

# Ordering Information

**TABLE 1. Package Marking and Ordering Information**

Output Voltage	Order Number	Package Type	Package Marking	Supplied As:
1.8	LP38512TJ-1.8	TO263-5 THIN	LP38512TJ-1.8	Rail
	LP38512TJX-1.8	TO263-5 THIN	LP38512TJ-1.8	Tape and Reel
	LP38512TS-1.8	TO263-5	LP38512TS-1.8	Rail
	LP38512TSX-1.8	TO263-5	LP38512TS-1.8	Tape and Reel

## Connection Diagrams



## Pin Descriptions for TO-263 and TO-263 THIN Packages

Pin #	Pin Name	Function
1	EN	Enable. Pull high to enable the output, low to disable the output. This pin has no internal bias and must be tied to the input voltage, or actively driven.
2	IN	Input Supply Pin
3	GND	Ground
4	OUT	Regulated Output Voltage Pin
5	$\overline{\text{ERROR}}$	$\overline{\text{ERROR}}$ Flag. A high level indicates that $V_{\text{OUT}}$ is within typically 15% ( $V_{\text{OUT}}$ falling) of the nominal regulated voltage.
TAB/DAP	TAB/DAP	The TO-263 TAB, and the TO-263 THIN DAP, is used as a thermal connection to remove heat from the device to an external heatsink. The TAB/DAP is internally connected to device pin 3, and is electrical ground connection.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	-65°C to +150°C
Soldering Temperature (Note 3)	
TO-220, Wave	260°C, 10s
TO-263	235°C, 30s
ESD Rating (Note 2)	±2 kV
Power Dissipation (Note 4)	Internally Limited
Input Pin Voltage (Survival)	-0.3V to +6.0V
Enable Pin Voltage (Survival)	-0.3V to +6.0V
Output Pin Voltage (Survival)	-0.3V to +6.0V
$\overline{\text{ERROR}}$ Pin Voltage (Survival)	0.3V to +6.0V
$I_{\text{OUT}}$ (Survival)	Internally Limited

**Operating Ratings** (Note 1)

Input Supply Voltage, $V_{\text{IN}}$	2.25V to 5.5V
Enable Input Voltage, $V_{\text{EN}}$	0.0V to 5.5V
$\overline{\text{ERROR}}$ Pin Voltage	0.0V to $V_{\text{IN}}$
Output Current (DC)	0 mA to 1.5A
Junction Temperature (Note 4)	-40°C to +125°C

**Electrical Characteristics**

Unless otherwise specified:  $V_{\text{IN}} = 2.5\text{V}$ ,  $I_{\text{OUT}} = 10\text{ mA}$ ,  $C_{\text{IN}} = 10\text{ }\mu\text{F}$ ,  $C_{\text{OUT}} = 10\text{ }\mu\text{F}$ ,  $V_{\text{EN}} = V_{\text{IN}}$ . Limits in standard type are for  $T_{\text{J}} = 25^\circ\text{C}$  only; limits in **boldface type** apply over the junction temperature ( $T_{\text{J}}$ ) range of  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ . Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at  $T_{\text{J}} = 25^\circ\text{C}$ , and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{\text{OUT}}$	Output Voltage Tolerance (Note 7)	$2.25\text{V} \leq V_{\text{IN}} \leq 5.5\text{V}$ $10\text{ mA} \leq I_{\text{OUT}} \leq 1.5\text{A}$	-1.0 <b>-2.5</b>	0	+1.0 <b>+2.5</b>	%
$\Delta V_{\text{OUT}}/\Delta V_{\text{IN}}$	Output Voltage Line Regulation (Notes 5, 7)	$2.25\text{V} \leq V_{\text{IN}} \leq 5.5\text{V}$	-	0.02 <b>0.06</b>	-	%/V
$\Delta V_{\text{OUT}}/\Delta I_{\text{OUT}}$	Output Voltage Load Regulation (Notes 6, 7)	$10\text{ mA} \leq I_{\text{OUT}} \leq 1.5\text{A}$	-	0.25 <b>0.40</b>	-	%/A
$V_{\text{DO}}$	Dropout Voltage (Note 8)	$I_{\text{OUT}} = 1.5\text{A}$	-	250	340 <b>400</b>	mV
$I_{\text{GND}}$	Ground Pin Current, Output Enabled	$I_{\text{OUT}} = 10\text{ mA}$ $\overline{\text{ERROR}}$ pin = GND	-	7.5	11 <b>12</b>	mA
		$I_{\text{OUT}} = 1.5\text{A}$ $\overline{\text{ERROR}}$ pin = GND	-	9.5	13 <b>14</b>	
	Ground Pin Current, Output Disabled	$V_{\text{EN}} = 0.50\text{V}$ $\overline{\text{ERROR}}$ pin = GND	-	0.1	3.5 <b>12</b>	$\mu\text{A}$
$I_{\text{SC}}$	Short Circuit Current	$V_{\text{OUT}} = 0\text{V}$	-	2.5	-	A

**Enable Input**

$V_{\text{EN(ON)}}$	Enable ON Threshold	$V_{\text{EN}}$ rising from 0.50V until $V_{\text{OUT}} = \text{ON}$	0.90 <b>0.80</b>	1.20	1.50 <b>1.60</b>	V
$V_{\text{EN(OFF)}}$	Enable OFF Threshold	$V_{\text{EN}}$ falling from 1.60V until $V_{\text{OUT}} = \text{OFF}$	0.60 <b>0.50</b>	1.00	1.40 <b>1.50</b>	
$V_{\text{EN(HYS)}}$	Enable Hysteresis	$V_{\text{EN(ON)}} - V_{\text{EN(OFF)}}$	-	200	-	mV
$t_{\text{d(OFF)}}$	Turn-off delay	Time from $V_{\text{EN}} < V_{\text{EN(OFF)}}$ to $V_{\text{OUT}} = \text{OFF}$ , $I_{\text{LOAD}} = 1.5\text{A}$	-	1	-	$\mu\text{s}$
$t_{\text{d(ON)}}$	Turn-on delay	Time from $V_{\text{EN}} > V_{\text{EN(ON)}}$ to $V_{\text{OUT}} = \text{ON}$ , $I_{\text{LOAD}} = 1.5\text{A}$	-	25	-	
$I_{\text{EN}}$	Enable Pin Current	$V_{\text{EN}} = V_{\text{IN}}$	-	1	-	nA
		$V_{\text{EN}} = 0\text{V}$	-	-1	-	

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>ERROR Flag</b>						
$V_{TH}$	Error Flag Threshold (Note 9)	$V_{OUT}$ rising threshold where $\overline{ERROR}$ Flag goes high	<b>78</b>	90	<b>98</b>	%
		$V_{OUT}$ falling threshold where $\overline{ERROR}$ Flag goes low	<b>74</b>	85	<b>93</b>	
$V_{ERROR(SAT)}$	ERROR Flag Saturation Voltage	$I_{SINK} = 100 \mu A$	-	12.5	<b>45</b>	mV
$I_{IK}$	ERROR Flag Pin Leakage Current	$V_{ERROR} = 5.5V$	-	1	-	nA
$t_d$	ERROR Flag Delay time		-	1	-	$\mu s$
<b>AC Parameters</b>						
PSRR	Ripple Rejection	$V_{IN} = 2.5V$ $f = 120Hz$	-	73	-	dB
		$V_{IN} = 2.5V$ $f = 1 kHz$	-	73	-	
$e_n$	Output Noise Density	$f = 120Hz$	-	2	-	$nV/\sqrt{Hz}$
	Output Noise Voltage	$BW = 100Hz - 100kHz$	-	75	-	$\mu V (RMS)$
<b>Thermal Characteristics</b>						
$T_{SD}$	Thermal Shutdown	$T_J$ rising	-	165	-	$^{\circ}C$
$\Delta T_{SD}$	Thermal Shutdown Hysteresis	$T_J$ falling from $T_{SD}$	-	10	-	
$\theta_{J-A}$	Thermal Resistance Junction to Ambient (Note 4)	TO-263 and TO-263 THIN	-	60	-	$^{\circ}C/W$
$\theta_{J-C}$	Thermal Resistance Junction to Case	TO-263 and TO-263 THIN	-	3	-	$^{\circ}C/W$

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and conditions, see the Electrical Characteristics.

**Note 2:** The human body model is a 100pF capacitor discharged through a 1.5k $\Omega$  resistor into each pin. Test method is per JESD22-A114.

**Note 3:** Refer to JEDEC J-STD-020C for surface mount device (SMD) package reflow profiles and conditions. Unless otherwise stated, the temperatures and times are for Sn-Pb (STD) only.

**Note 4:** Device operation must be evaluated, and derated as needed, based on ambient temperature ( $T_A$ ), power dissipation ( $P_D$ ), maximum allowable operating junction temperature ( $T_{J(MAX)}$ ), and package thermal resistance ( $\theta_{JA}$ ).

**Note 5:** Output voltage line regulation is defined as the change in output voltage from the nominal value ( $\Delta V_{OUT}$ ) due to a change in the voltage at the input ( $\Delta V_{IN}$ ).

**Note 6:** Output voltage load regulation is defined as the change in output voltage from the nominal value ( $\Delta V_{OUT}$ ) due to a change in the load current at the output ( $\Delta I_{OUT}$ ).

**Note 7:** The line and load regulation specification contains only the typical number. However, the limits for line and load regulation are included in the output voltage tolerance specification.

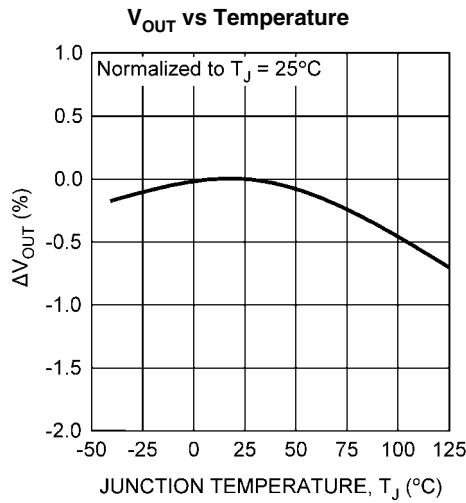
**Note 8:** Dropout voltage is defined as the minimum input to output differential voltage at which the output drops 2% below the nominal value. For the LP38512-1.8 the minimum  $V_{IN}$  operating voltage is the limiting factor.

**Note 9:** The  $\overline{ERROR}$  Flag thresholds are specified as percentage of the nominal regulated output voltage. See Application Information.

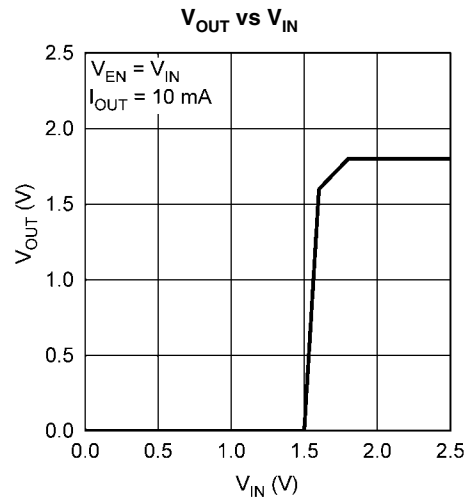
# Typical Performance Characteristics

Unless otherwise specified:  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = 2.5\text{V}$ ,  $V_{EN} = V_{IN}$ ,

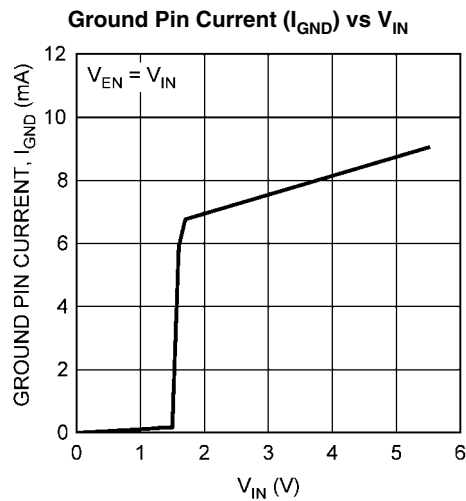
$C_{IN} = 10\ \mu\text{F}$ ,  $C_{OUT} = 10\ \mu\text{F}$ ,  $I_{OUT} = 10\ \text{mA}$ .



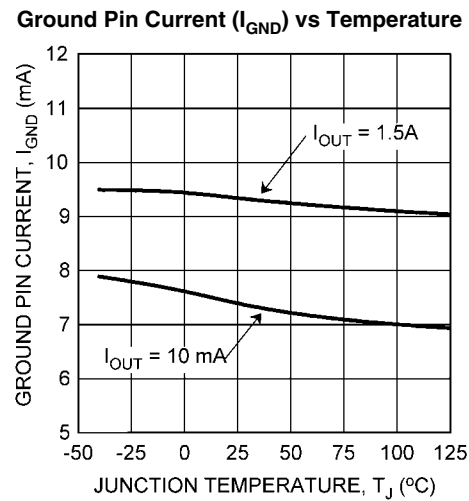
20183011



20183037

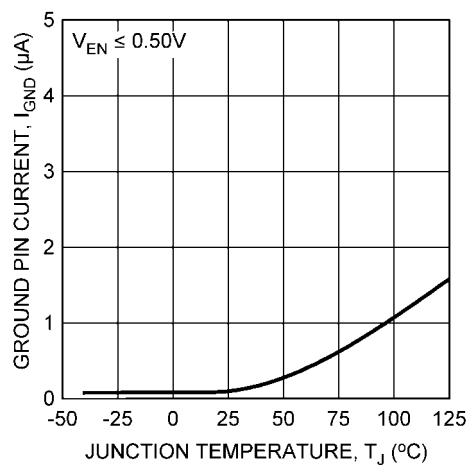


20183012



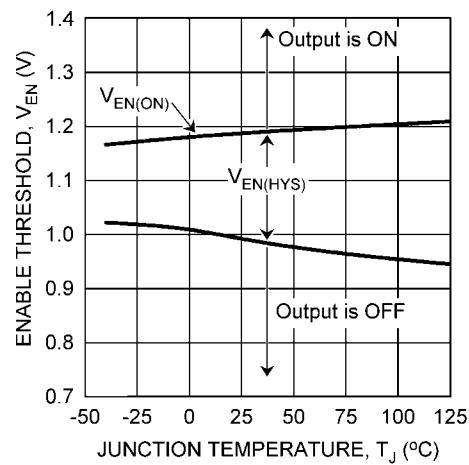
20183013

### Ground Pin Current ( $I_{GND}$ ) vs Temperature, $V_{EN} = 0.5\text{V}$

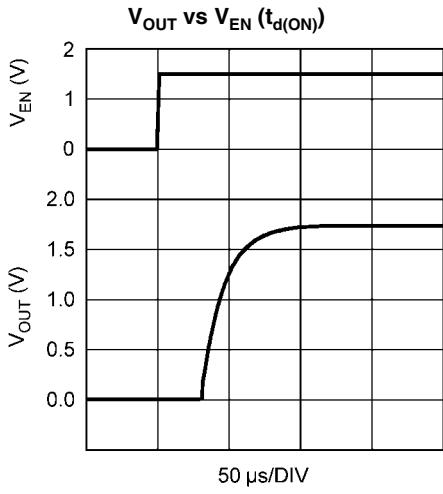


20183014

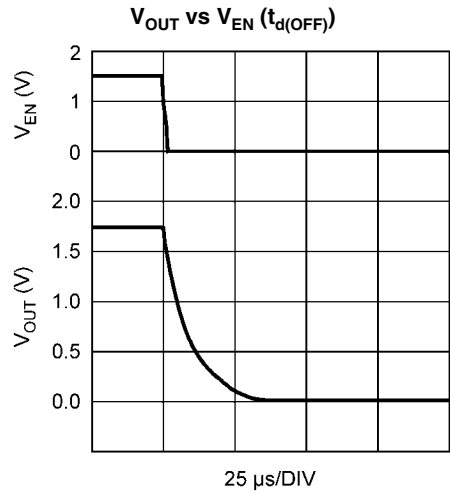
### Enable Thresholds vs Temperature



20183016

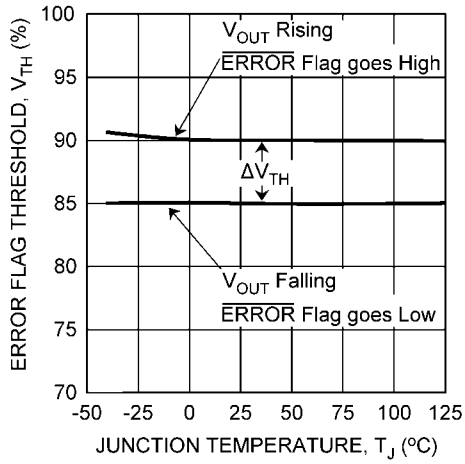


20183032



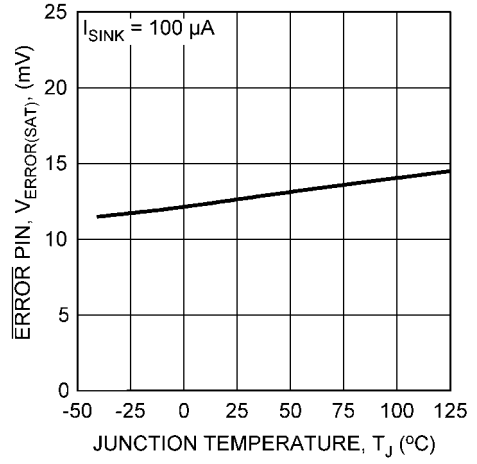
20183030

### V<sub>OUT</sub> ERROR Flag Threshold vs Temperature



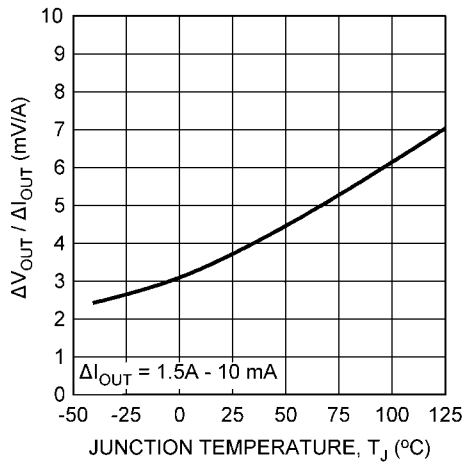
20183017

### ERROR Flag Low vs Temperature



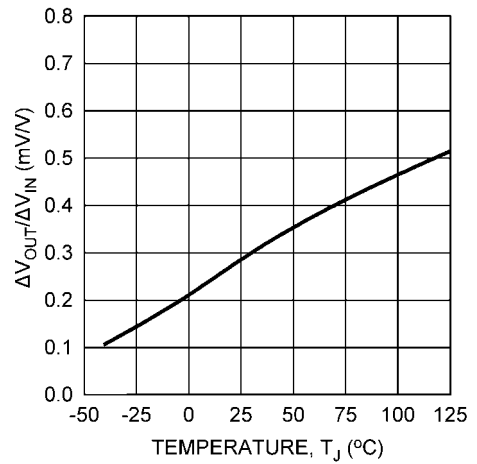
20183018

### Load regulation vs Temperature

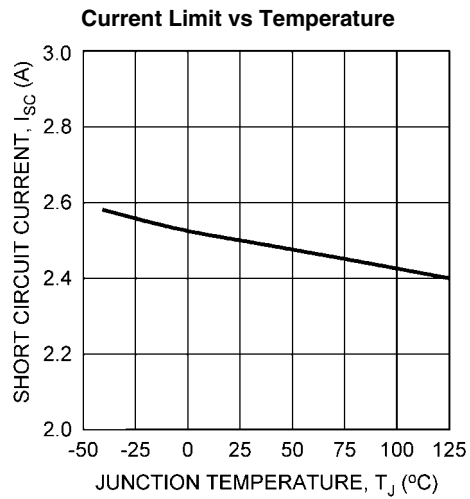


20183020

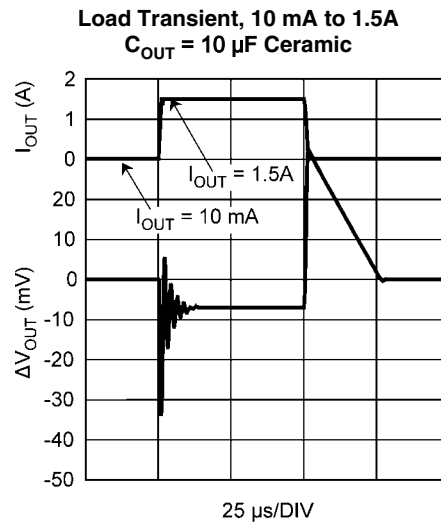
### Line Regulation vs Temperature



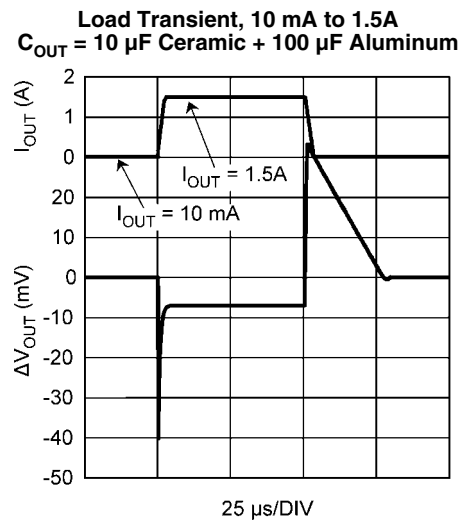
20183021



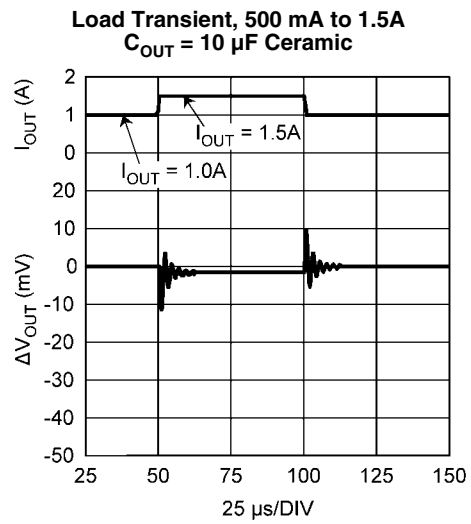
20183022



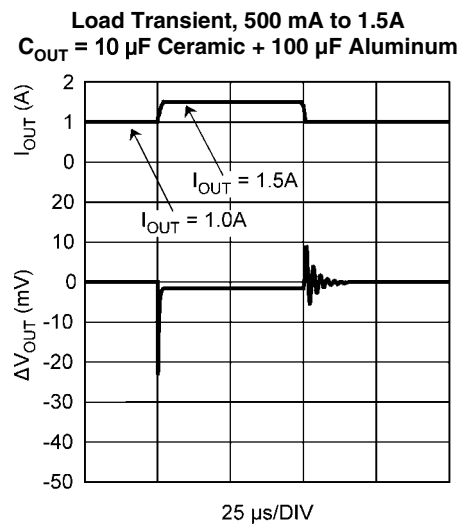
20183023



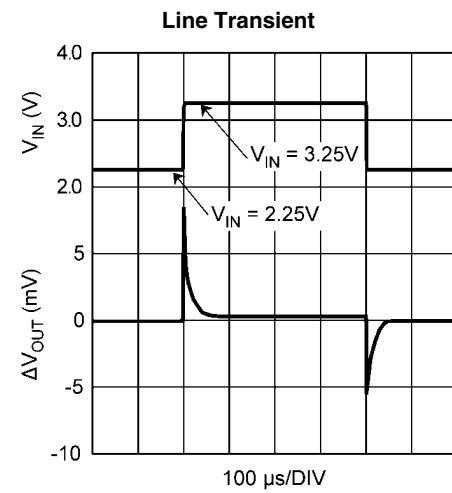
20183024



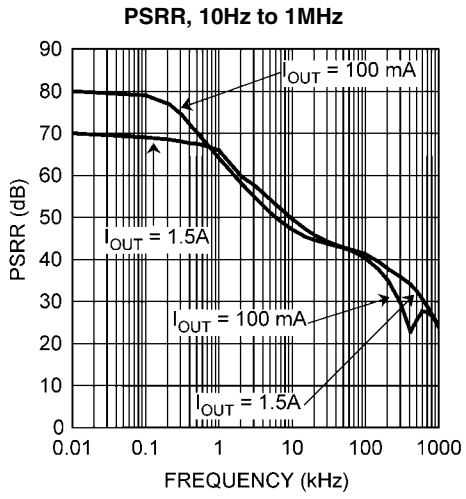
20183025



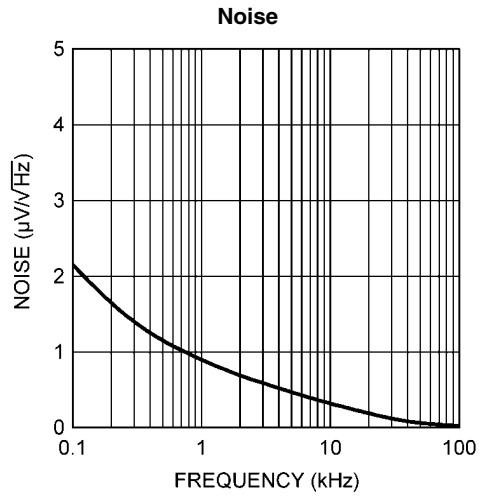
20183026



20183027



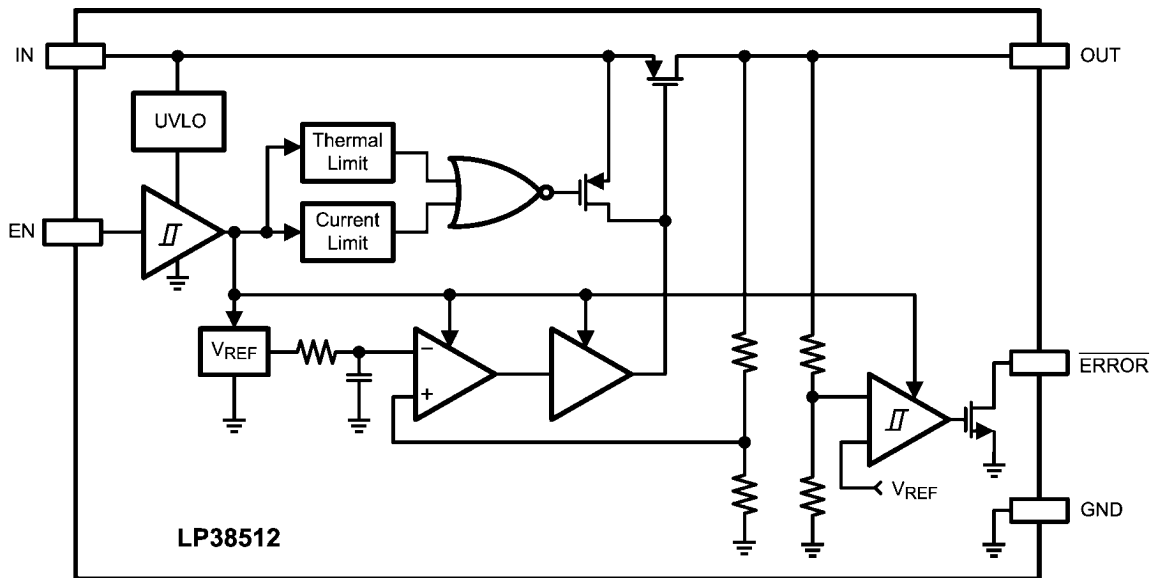
20183029



20183031



## Block Diagram



20183007

## Application Information

### EXTERNAL CAPACITORS

Like any low-dropout regulator, external capacitors are required to assure stability. These capacitors must be correctly selected for proper performance.

#### Input Capacitor

A ceramic input capacitor of at least 10  $\mu\text{F}$  is required. For general usage across all load currents and operating conditions, a 10  $\mu\text{F}$  ceramic input capacitor will provide satisfactory performance.

#### Output Capacitor

A ceramic capacitor with a minimum value of 10  $\mu\text{F}$  is required at the output pin for loop stability. It must be located less than 1 cm from the device and connected directly to the output and ground pin using traces which have no other currents flowing through them. As long as the minimum of 10  $\mu\text{F}$  ceramic is met, there is no limitation on any additional capacitance.

X7R and X5R dielectric ceramic capacitors are strongly recommended, as they typically maintain a capacitance range within  $\pm 20\%$  of nominal over full operating ratings of temperature and voltage. Of course, they are typically larger and more costly than Z5U/Y5U types for a given voltage and capacitance.

Z5U and Y5V dielectric ceramics are not recommended as the capacitance will drop severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it. The Z5U and Y5V also exhibit a severe temperature effect, losing more than 50% of nominal capacitance at high and low limits of the temperature range.

### REVERSE VOLTAGE

A reverse voltage condition will exist when the voltage at the output pin is higher than the voltage at the input pin. Typically this will happen when  $V_{\text{IN}}$  is abruptly taken low and  $C_{\text{OUT}}$  continues to hold a sufficient charge such that the input to output

voltage becomes reversed. A less common condition is when an alternate voltage source is connected to the output.

There are two possible paths for current to flow from the output pin back to the input during a reverse voltage condition.

While  $V_{\text{IN}}$  is high enough to keep the control circuitry alive, and the Enable pin is above the  $V_{\text{EN(ON)}}$  threshold, the control circuitry will attempt to regulate the output voltage. Since the input voltage is less than the output voltage the control circuit will drive the gate of the pass element to the full on condition when the output voltage begins to fall. In this condition, reverse current will flow from the output pin to the input pin, limited only by the  $R_{\text{DS(ON)}}$  of the pass element and the output to input voltage differential. Discharging an output capacitor up to 1000  $\mu\text{F}$  in this manner will not damage the device as the current will rapidly decay. However, continuous reverse current should be avoided.

The internal PFET pass element in the LP38512 has an inherent parasitic diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, if the output voltage to input voltage differential is more than 500 mV (typical) the parasitic diode becomes forward biased and current flows from the output pin to the input through the diode. The current in the parasitic diode should be limited to less than 1A continuous and 5A peak.

If used in a dual-supply system where the regulator output load is returned to a negative supply, the output pin must be diode clamped to ground. A Schottky diode is recommended for this protective clamp.

### SHORT-CIRCUIT PROTECTION

The LP38512 is short circuit protected, and in the event of a peak over-current condition the short-circuit control loop will rapidly drive the output PMOS pass element off. Once the power pass element shuts down, the control loop will rapidly cycle the output on and off until the average power dissipation causes the thermal shutdown circuit to respond to servo the

on/off cycling to a lower frequency. Please refer to the *POWER DISSIPATION/HEATSINKING* section for power dissipation calculations.

**ENABLE OPERATION**

The Enable ON threshold is typically 1.2V, and the OFF threshold is typically 1.0V. To ensure reliable operation the Enable pin voltage must rise above the maximum  $V_{EN(ON)}$  threshold and must fall below the minimum  $V_{EN(OFF)}$  threshold. The Enable threshold has typically 200mV of hysteresis to improve noise immunity.

The Enable pin (EN) has no internal pull-up or pull-down to establish a default condition and, as a result, this pin must be terminated either actively or passively.

If the Enable pin is driven from a single ended device (such as discrete transistor) a pull-up resistor to  $V_{IN}$ , or a pull-down resistor to ground, will be required for proper operation. A 1 k $\Omega$  to 100 k $\Omega$  resistor can be used as the pull-up or pull-down resistor to establish default condition for the EN pin. The resistor value selected should be appropriate to swamp out any leakage in the external single ended device, as well as any stray capacitance.

If the Enable pin is driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator output), the pull-up, or pull-down, resistor is not required.

If the application does not require the Enable function, the pin should be connected to directly to the adjacent  $V_{IN}$  pin.

The status of the Enable pin also affects the behavior of the ERROR Flag. While the Enable pin is high the regulator con-

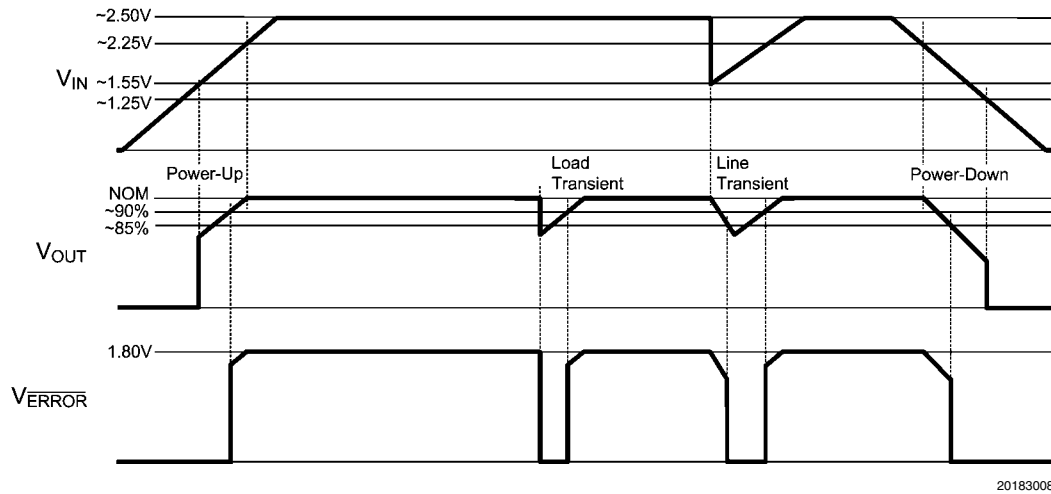
trol loop will be active and the  $\overline{ERROR}$  Flag will report the status of the output voltage. When the Enable pin is taken low the regulator control loop is shutdown, the output is turned off, and the ERROR Flag pin is immediately forced low.

**ERROR FLAG OPERATION**

When the LP38512 Enable pin is high, the  $\overline{ERROR}$  Flag pin will produce a logic low signal when the output drops by more than 15% (typical) from the nominal output voltage. The drop in output voltage may be due to low input voltage, current limiting, or thermal limiting. This flag has a built in hysteresis. The output voltage will need to rise to within 10% (typical) of the nominal output voltage for the ERROR Flag to return to a logic high state. It should also be noted that when the Enable pin is pulled low, the  $\overline{ERROR}$  Flag pin is forced to be low as well.

The internal  $\overline{ERROR}$  flag comparator has an open drain output stage. Hence, the  $\overline{ERROR}$  pin requires an external pull-up resistor. The value of the pull-up resistor should be in the range of 10 k $\Omega$  to 1 M $\Omega$ . The  $\overline{ERROR}$  Flag pin should not be pulled-up to any voltage source higher than  $V_{IN}$  as current flow through an internal parasitic diode may cause unexpected behavior. The  $\overline{ERROR}$  Flag must be connected to ground if this function is not used.

The timing diagram in *Figure 1* shows the relationship between the  $\overline{ERROR}$  flag and the output voltage.



**FIGURE 1.  $\overline{ERROR}$  Flag Operation, see Typical Application**

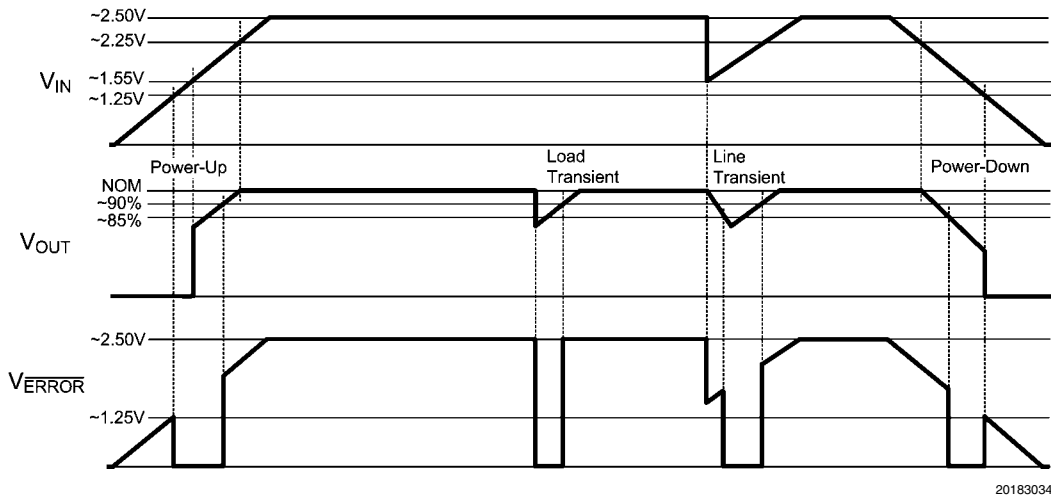


FIGURE 2. ERROR Flag Operation, biased from  $V_{IN}$

**POWER DISSIPATION/HEATSINKING**

A heatsink may be required depending on the maximum power dissipation ( $P_{D(MAX)}$ ), maximum ambient temperature ( $T_{A(MAX)}$ ) of the application, and the thermal resistance ( $\theta_{JA}$ ) of the package. Under all possible conditions, the junction temperature ( $T_J$ ) must be within the range specified in the Operating Ratings. The total power dissipation of the device is given by:

$$P_D = ((V_{IN} - V_{OUT}) \times I_{OUT}) + (V_{IN} \times I_{GND}) \quad (1)$$

where  $I_{GND}$  is the operating ground current of the device (specified under Electrical Characteristics).

The maximum allowable junction temperature rise ( $\Delta T_J$ ) depends on the maximum expected ambient temperature ( $T_{A(MAX)}$ ) of the application, and the maximum allowable junction temperature ( $T_{J(MAX)}$ ):

$$\Delta T_J = T_{J(MAX)} - T_{A(MAX)} \quad (2)$$

The maximum allowable value for junction to ambient Thermal Resistance,  $\theta_{JA}$ , can be calculated using the formula:

$$\theta_{JA} = \Delta T_J / P_{D(MAX)} \quad (3)$$

**HEATSINKING TO-263 PACKAGE**

The TO-263 and the TO-263 THIN packages use the copper plane on the PCB as a heatsink. The tab, or DAP, of these packages are soldered to the copper plane for heat sinking. Figure 3 shows a curve for the  $\theta_{JA}$  of TO-263 package for different copper area sizes, using a typical PCB with 1 ounce copper and no solder mask over the copper area for heat sinking.

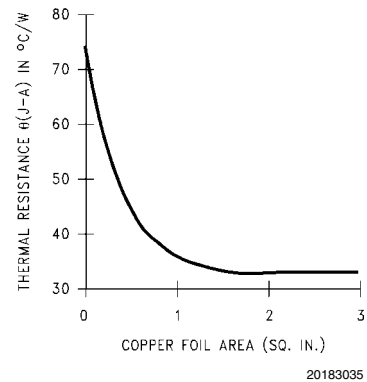


FIGURE 3.  $\theta_{JA}$  vs Copper (1 Ounce) Area for TO-263 package

As shown in the figure, increasing the copper area beyond 1 square inch produces very little improvement. The minimum value for  $\theta_{JA}$  for the TO-263 package mounted to a two-layer PCB is 32°C/W.

Figure 4 shows the maximum allowable power dissipation for TO-263 packages for different ambient temperatures, assuming  $\theta_{JA}$  is 35°C/W and the maximum junction temperature is 125°C.

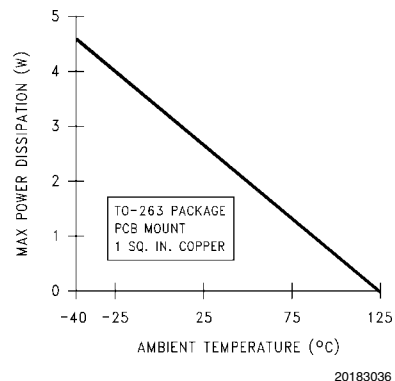
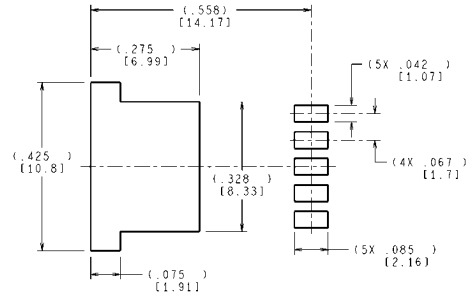
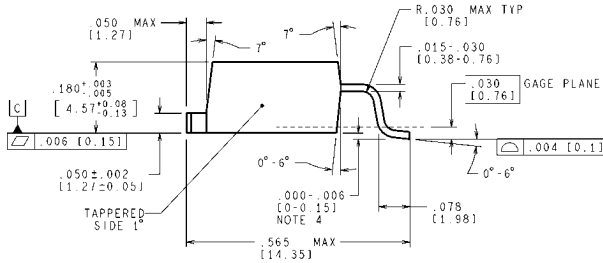
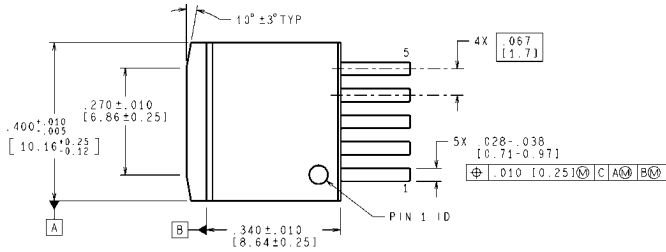
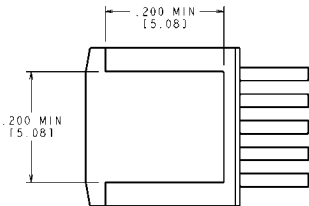


FIGURE 4. Maximum Power Dissipation vs Ambient Temperature for TO-263 Package

**Physical Dimensions** inches (millimeters) unless otherwise noted



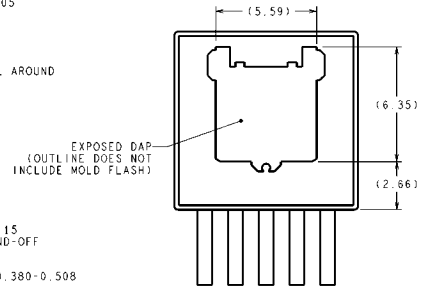
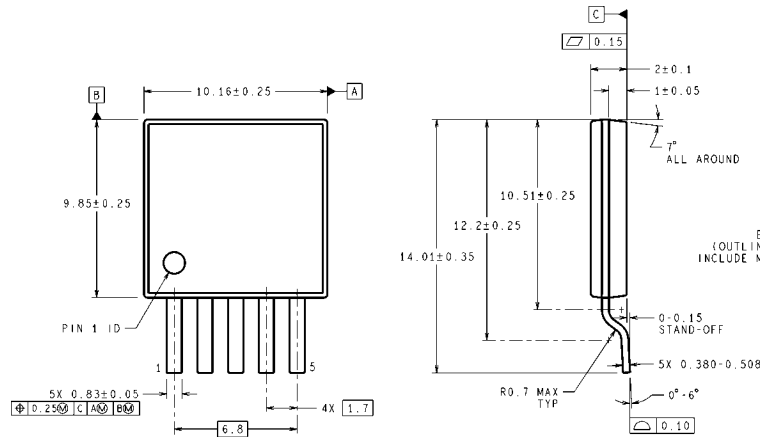
LAND PATTERN RECOMMENDATION



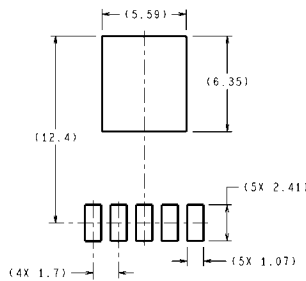
CONTROLLING DIMENSION IS INCH  
VALUES IN [ ] ARE MILLIMETERS  
DIMENSIONS IN ( ) FOR REFERENCE ONLY

**TO-263, Molded, 5-Lead, 0.067in (1.7mm) Pitch, Surface Mount Package  
NS Package Number TS5B**

TS5B (Rev D)



DIMENSIONS ARE IN MILLIMETERS  
DIMENSIONS IN ( ) FOR REFERENCE ONLY



RECOMMENDED LAND PATTERN

**TO-263 THIN, Molded, 5-Lead, 1.7mm Pitch, Surface Mount Package  
NS Package Number TJ5A**

TJ5A (Rev E)

# Notes

LP38512-1.8

## Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

Products		Design Support	
Amplifiers	<a href="http://www.national.com/amplifiers">www.national.com/amplifiers</a>	WEBENCH	<a href="http://www.national.com/webench">www.national.com/webench</a>
Audio	<a href="http://www.national.com/audio">www.national.com/audio</a>	Analog University	<a href="http://www.national.com/AU">www.national.com/AU</a>
Clock Conditioners	<a href="http://www.national.com/timing">www.national.com/timing</a>	App Notes	<a href="http://www.national.com/appnotes">www.national.com/appnotes</a>
Data Converters	<a href="http://www.national.com/adc">www.national.com/adc</a>	Distributors	<a href="http://www.national.com/contacts">www.national.com/contacts</a>
Displays	<a href="http://www.national.com/displays">www.national.com/displays</a>	Green Compliance	<a href="http://www.national.com/quality/green">www.national.com/quality/green</a>
Ethernet	<a href="http://www.national.com/ethernet">www.national.com/ethernet</a>	Packaging	<a href="http://www.national.com/packaging">www.national.com/packaging</a>
Interface	<a href="http://www.national.com/interface">www.national.com/interface</a>	Quality and Reliability	<a href="http://www.national.com/quality">www.national.com/quality</a>
LVDS	<a href="http://www.national.com/lvds">www.national.com/lvds</a>	Reference Designs	<a href="http://www.national.com/refdesigns">www.national.com/refdesigns</a>
Power Management	<a href="http://www.national.com/power">www.national.com/power</a>	Feedback	<a href="http://www.national.com/feedback">www.national.com/feedback</a>
Switching Regulators	<a href="http://www.national.com/switchers">www.national.com/switchers</a>		
LDOs	<a href="http://www.national.com/ldo">www.national.com/ldo</a>		
LED Lighting	<a href="http://www.national.com/led">www.national.com/led</a>		
PowerWise	<a href="http://www.national.com/powerwise">www.national.com/powerwise</a>		
Serial Digital Interface (SDI)	<a href="http://www.national.com/sdi">www.national.com/sdi</a>		
Temperature Sensors	<a href="http://www.national.com/tempsensors">www.national.com/tempsensors</a>		
Wireless (PLL/VCO)	<a href="http://www.national.com/wireless">www.national.com/wireless</a>		

THE CONTENTS OF THIS DOCUMENT ARE PROVIDED IN CONNECTION WITH NATIONAL SEMICONDUCTOR CORPORATION ("NATIONAL") PRODUCTS. NATIONAL MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE ACCURACY OR COMPLETENESS OF THE CONTENTS OF THIS PUBLICATION AND RESERVES THE RIGHT TO MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. NO LICENSE, WHETHER EXPRESS, IMPLIED, ARISING BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

TESTING AND OTHER QUALITY CONTROLS ARE USED TO THE EXTENT NATIONAL DEEMS NECESSARY TO SUPPORT NATIONAL'S PRODUCT WARRANTY. EXCEPT WHERE MANDATED BY GOVERNMENT REQUIREMENTS, TESTING OF ALL PARAMETERS OF EACH PRODUCT IS NOT NECESSARILY PERFORMED. NATIONAL ASSUMES NO LIABILITY FOR APPLICATIONS ASSISTANCE OR BUYER PRODUCT DESIGN. BUYERS ARE RESPONSIBLE FOR THEIR PRODUCTS AND APPLICATIONS USING NATIONAL COMPONENTS. PRIOR TO USING OR DISTRIBUTING ANY PRODUCTS THAT INCLUDE NATIONAL COMPONENTS, BUYERS SHOULD PROVIDE ADEQUATE DESIGN, TESTING AND OPERATING SAFEGUARDS.

EXCEPT AS PROVIDED IN NATIONAL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NATIONAL ASSUMES NO LIABILITY WHATSOEVER, AND NATIONAL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF NATIONAL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

### LIFE SUPPORT POLICY

**NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION.** As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

National Semiconductor and the National Semiconductor logo are registered trademarks of National Semiconductor Corporation. All other brand or product names may be trademarks or registered trademarks of their respective holders.

Copyright© 2008 National Semiconductor Corporation

For the most current product information visit us at [www.national.com](http://www.national.com)



**National Semiconductor Americas Technical Support Center**  
 Email: [support@nsc.com](mailto:support@nsc.com)  
 Tel: 1-800-272-9959

**National Semiconductor Europe Technical Support Center**  
 Email: [europe.support@nsc.com](mailto:europe.support@nsc.com)  
 German Tel: +49 (0) 180 5010 771  
 English Tel: +44 (0) 870 850 4288

**National Semiconductor Asia Pacific Technical Support Center**  
 Email: [ap.support@nsc.com](mailto:ap.support@nsc.com)

**National Semiconductor Japan Technical Support Center**  
 Email: [jpn.feedback@nsc.com](mailto:jpn.feedback@nsc.com)